National Semiconductor

Bipolar PROMs

DM54S474/DM74S474 4096-Bit (512 × 8) TRI-STATE® PROM DM54S475/DM74S475 4096-Bit (512 × 8) **Open-Collector PROM**

general description

These Schottky memories are organized in the popular 512 words by 8 bits configuration. Four memory enable inputs are provided to control the output states. When E1 and E2 are low and E3 and E4 are high, the output presents the contents of the selected word.

If E1 or E2 are high, or E3 or E4 are low, it causes all 8 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as ROM's as well as PROM's.

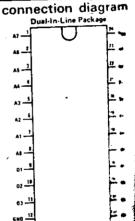
PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

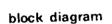
See page 5-36 of the Memory Applications Handbook for detailed programming information.

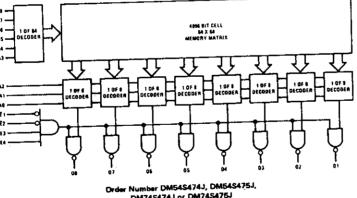
features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed Address access-65 ns Enable access-35 ns
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFETM programming
- Board level programming
- ROM mates are DM87S95 and DM87S96

	Military	Commercial	Open- Collector	TRI-STATE	Package
DM74S475		×	×		N, J
DM745474	 	×		×	N, J
	 -;		X		J
DM54S475	 			×	J

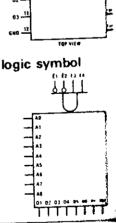






DM74S474J or DM74S476J Can NS Package J24A

Order Number DM74S474N or DM74S475N See NS Package N24B



6

absolute maximum	ratings	(Note 1)
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Supply Voltage (Note 2) Input Voltage (Note 2) Output Voltage (Note 2) Storage Temperature Lead Temperature (Soldering, 10 seconds)	~0.5V to +7V ~1.2V to +5.5V ~0.5V to +5.5V ~65°C to +150°C
(Soldering, 10 seconds)	300°C

operating conditions

Supply Voltage (VCC)	MiN	MAX	UNIT
DM54S474, DM54S475 DM74S474, DM74S475	4.5 4.75	5.5 5.25	٧
Ambient Temperature (TA)			•
DM54S474, DM54S475 DM74S474, DM74S475	55 0	+125	°c
Logical "0" Input Voltage (Low)	0	+70 0.8	°C
Logical "1" Input Voltage (High)	2.0	5.5	V

dc electrical characteristics (Note 3)

PARAMETER	CONDITIONS	DM5	DM54S474, DM54S475				DM74S474, DM74S475		
Input Load Current, All Inputs	† V	MIN	TYP	MAX				UNIT	
Input Leakage Current, All Inpu	VCC = Max, VIN = 0.45V		-80	-250		-80	-250	μА	
Input Leakage Current, All Inpu				25	1	_	25	 	
Low Level Output Voltage				1.0	+	 -	1.0	μΑ	
	VCC = Min, IQL = 16 mA	7	0.35	0.5	+	0.35	+ ~~	mA	
Low Level Input Voltage		 	 	0.80	┼	0.35	+		
High Level Input Voltage		2.0	 	0.80	┼	 	0.80	V	
Output Leakage Current	V _{CC} = Max, V _{CEX} = 2.4V	1		<u> </u>	2.0			v	
(Open-Collector Only) (Note 5)	V _{CC} = Max, V _{CEX} = 5.5V	 		50	_	<u> </u>	50	μА	
Input Clamp Voltage	VCC = Min, I;N = ~18 mA	 		100	├	ــــ	100	μА	
Input Capacitance	VCC = 5V, VIN = 2V, TA = 25°C,	{	-0.8	-1.2	<u> </u>	-0.8	-1.2	V	
	1 MHz	1 1	4.0		}	4.0	1 7	ρF	
Output Capacitance	VCC = 5V, VO = 2V, T _A = 25°C, 1 MHz, Output "OFF"	 	6.0			6.0		pF	
Power Supply Current	VCC = Max, All Inputs Grounded, All Outputs Open	 - 	115	170		115	170	mA	
ATE PARAMETERS		<u> </u>						""	
Output Short Circuit Current	Vo = 0V, VCC = Max, (Note 4)								
(Note 5)	TO UV, VCC * Max, (Note 4)	-20	1	-70	-20		-70	mA	
Output Leakage (TRI-STATE)	V _{CC} = Max, V _O = 0.45 to 2.4V,						1		
·	Chip Disabled	- 1	ŀ	±50			±50	μA	
Output Voltage High, (Note 5)	IOH = -2.mA						1		
<u>s'</u>	OH = 6.5 mA	2.4	3.2		-I	T		v	
			- 1	- i	2.4	3.2			

lectrical characteristics (With standard load)

PARAMETER	CONDITIONS		DM54S474, DM54S475 SV ±10%;~55°C to +125°C					
dress Access Time	(Figure 1)	MiN	TYP	MAX	MIN	TYP	MAX	UNITS
able Access Time	(Figure 2)		40	75		40	65	пѕ
ble Recovery Time	(Figure 2)		20	40		20	35	ns
L S	e those values beyond which the desir		20	40	•	20	35	ns

Debute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device

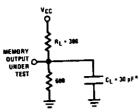
limits do not apply during programming. For the programming ratings, refer to the programming instructions.

limits apply over the entire operating range unless stated otherwise. All typical values are for $V_{CC} = 5V$ and $T_A = 25^{\circ}C$.

ISC measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

ure VOH, ICEX or ISC on an unprogrammed part, apply 10.5V to both A7 and A2 (pin 1 and pin 6).

standard test load



*CL includes probe and jig capacitance.

- Input waveforms are supplied by a pulse generator having the following characteristics: PRR = 1 MHz, $Z_{OUT} = 50\Omega$, $t_r \le 2.5$ ns and $t_f \le 2.5$ ns (between 1.0V and 2.0V).
- tAA is measured with both enable inputs at a steady low level.
- tEA and tER are measured from the 1.5V on inputs and outputs with all address inputs at a steady level and with the unused enable input at a steady low level.

switching time waveforms

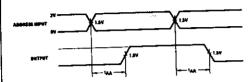


FIGURE 1. Address Access Time

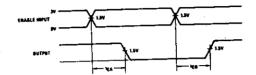
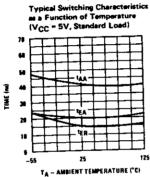
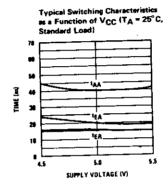


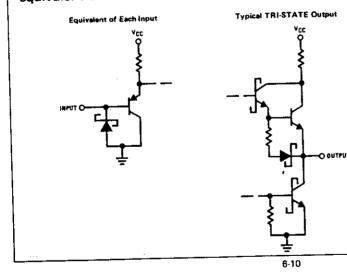
FIGURE 2. Enable Access Time and Recovery Time

typical performance characteristics





equivalent circuits



Typical Open-Collector Output



HM-7640A/41A

512 x 8 PROM

HM-7640A - Open Collector Outputs HM-7641A - "Three State" Outputs

APRIL 1978

Features

- 50m MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND FOUR CHIPS ENABLE INPUTS.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME GUARANTEED FOR WORST CASE N² SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- LOW INPUT LOADING

Description

The HM-7640A/41A are fully decoded high speed Schottky TTL 4096-Bit Field Programmable ROMs in a 512 word by 8 bit/word format and are available in a 24 pin DIP (ceramic or epoxy) and a 24 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on this and all other Harris Bipolar PROM's.

The HM-7640A/41A contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

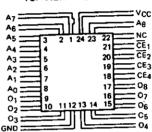
There are four chip enable inputs on the HM-7640A/41A where $\overline{\text{CE}}_1$, and $\overline{\text{CE}}_2$ low and CE3 and CE4 high enables the chip.

Pinouts

TOP VIEW - DIP



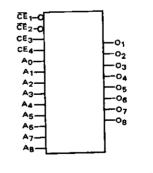
TOP VIEW -- FLATPACK

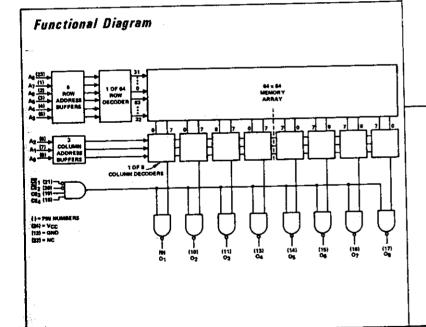


PIN NAMES

 $\begin{array}{c} A_0 = A_8 \quad \text{Address Inputs} \\ O_1 = O_8 \quad \text{Data Outputs} \\ \overline{\text{CE}}_1, \overline{\text{CE}}_2, \text{CE}_3, \text{CE}_4 \quad \text{Chip Enable Inputs} \end{array}$

Logic Symbol





Specifications HM-7640A/41A

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating) -0.3 to +7.0V Storage Temperature -65°C to +150°C Address/Enable Input Voltage 5.5V Operating Temperature (Ambient) -55°C to +125°C Address/Enable Input Current -20mA Maximum Junction Temperature +175°C Output Sink Current 100mA

CAUTION: Stresses above those listed under the "Absolute Maximum Retings" may cause permanent demage to the device. These are stress only retings and functional operation of the device at these or at any other conditions above those indicated in the operations sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7640A/41A-5 {V_{CC} = $5.0V \pm 5\%$, T_A = 0° C to +75°C) HM-7640A/41A-2 {V_{CC} = $5.0V \pm 10\%$, T_A = -55° C to +12 Typical measurements are at T_A = 25° C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
иг ин	Address/Enable "1" input Current "0"	_	 -50.0	+40 -250	μA μA	VIH = VCC Mex. VIL = 0.45V
VIH VIL	Input Threshold "1" Voltage "0"	2.0	1.5 1.5	0.8	V	VCC = VCC Min. VCC = VCC Max.
VOL.	Output "1" Voltage "0"	2.4*	3.2° 0.35	_ 0.45	V	IOH = -2.0mA, VCC = VCC Min. IOL = +16mA, VCC = VCC Min.
IOLE	Output Disable "1" Current "0"	-	-	+40 -40*	μΑ μΑ	VOH, VCC = VCC Max. VOL = 0.3V, VCC = VCC Max.
VCL	Input Clamp Voltage	-	-	-1.2	V	1 N = -18mA
los	Output Short Circuit Current	-15*		-100*	mA	VOUT = 0.0V, One Output at a Time for a Max, of 1 Second
Icc	Power Supply Current	-	125	170	mA	VCC = VCC Max., All Inputs Grounded,

NOTE: Positive current defined as into device terminals.

"'Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

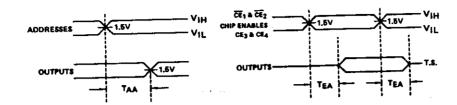
		HM-7640A/41A 5V ±5% 0°C to +75°C			HM-7640A/41A 5V ±10% -55°C to +125°C				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	
TAA	Address Access Time	_	35	. 50	-	-	70	ns.	
TEA	Chip Enable Access Time	-	30	40	-	_	50	ns	

A.C. limits guaranteed for worst case N² sequencing.

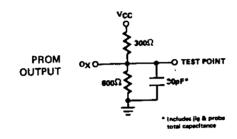
CAPACITANCE: TA = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
CINA, CINCE	Input Capacitance	8	pF	VCC = 5V, VIN = 2.0V, f = 1MHz
COUT	Output Capacitance	10	pF	VCC = 5V, VOUT = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS

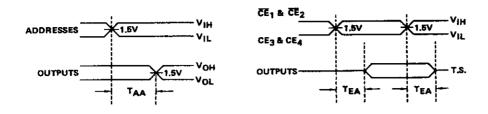


A.C. TEST LOAD

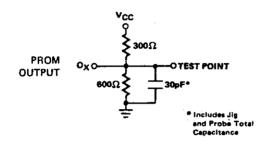


50C)

SWITCHING TIME DEFINITIONS



A.C. TEST LOAD





HM-7642A/43A

1K x 4 PROM

HM-7642A - Open Collector Outputs ► HM-7643A - "Three State" Outputs

MARCH 1978

- Features 50ns MAXIMUM ADDRESS ACCESS TIME.
 - "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND TWO CHIP
 - SIMPLE HIGH SPEED PROGRAMMING PROCEDURE ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILIT
 - FAST ACCESS TIME GUARANTEED FOR WORST CASE N2 SEQUENC-ING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLT-AGE RANGES.
 - AGE HANGES.
 INDUSTRY'S HIGHEST PROGRAMMING YIELD.

Description

The HM-7642A/43A are fully decoded high speed Schottky TTL 4096-Bit Field Programmable ROMs in a 1K words by 4 Bit/word format with open collector(HM-7642A) or "Three State" (HM-7643A) outputs. These open collector(HM-7642A) or "Three State" (FIM-700XY) and an 18—pin PROM's are available in an 18—pin DIP (ceramic or epoxy) and an 18—pin flat pack.

All bits are manufactured storing a logical "1" (positive logic) and can be electively programmed for a logical "0" in any bit position.

schrome fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7642A/43A contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee for the storage array to assure high programmability and guarantee. The fuses in these test rows and accompanies and A.C. performance. blumns are blown prior to shipment.

are two chip enable inputs on the HM-7642A/43A. \overrightarrow{CE}_1 and \overrightarrow{CE}_2 four enables the chip.

Pinout

TOP VIEW-DIP

A 6 □ 1	18 VCC
A5 2	17 🗖 🗛
A4 🛚 3	16 AB
A3 🛮 4	15 A9
A0 5	14 01
A1 6	13 02
A2 ☐ 7	12 03
⋶ 1 🖸 8	11 04
CND[]9	10 0 0 0 0 0 0 0 0

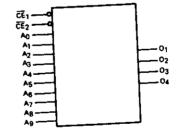
TOP VIEW-FLAT PACK

ayumma s	Automati Acc
A5 <u>22222227</u> 8A	CONTRACT AT
v* 7727772 3.5 1	18 17 16 CULTULE A8
A3 2222222 4 A0 2222222 5	14 ZZZZZZZ O1
A1 222222 6	13 ZZZZZZZ 02
* 8 VIIIII CA	10 1112 1111111111111111111111111111111
<u>CE</u> 2222222	Manager 04
GND MINIMUM	VIIIIIIIII OCA

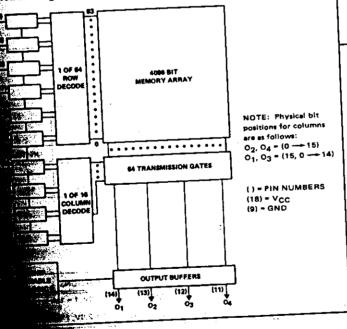
PIN NAMES

ADDRESS INPUTS A₀ - A₉ DATA OUTPUTS 01 - 04 CHIP ENABLE INPUTS ČĒ1, ČĒ2

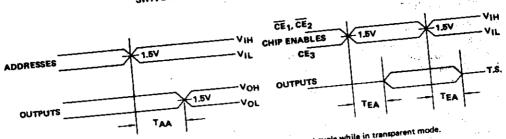
Logic Symbol



ectional Diagram

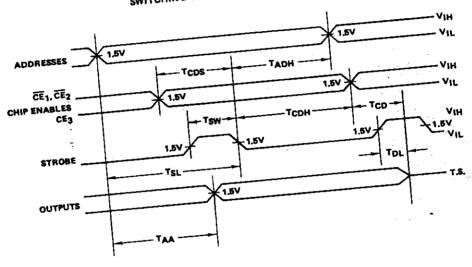


SWITCHING TIME DEFINITIONS (Transparent Mode)

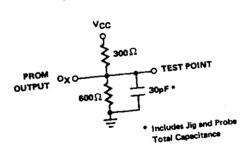


NOTE: Strobe input must remain high throughout read cycle while in transparent mode.

SWITCHING TIME DEFINITIONS (Latched Mode)



A.C. TEST LOAD



SCHOTTKY[†] PROM'S

SERIES 54S/74S PROGRAMMABLE READ-ONLY MEMORIES

- Titanium-Tungsten (Ti-W) Fuse Links for Fast, Low-Voltage, Reliable Programming
- All Schottky-Clamped PROM's Offer:

 Fast Chip Select to Simplify System Decode
 Choice of Three-State or Open-Collector Outputs
 P-N-P Inputs for Reduced Loading on
 System Buffers/Drivers
- Full Decoding and Chip Select Simplify System Design
 - Applications Include:
 Microprogramming/Firmware Loaders
 Code Converters/Character Generators
 Translators/Emulators
 Address Mapping/Look-Up Tables

TYPE NUMBER (PACKAGES)		BIT SIZE	OUTPUT	TYPICAL PERFORMANCE			
-55°C to 125°C	0°C to 70°C	(ORGANIZATION)	CONFIGURATION	ADDRESS ACCESS TIME	POWER DISSIPATION		
\$N 54\$188(J, W)	SN74S188(J, N)	256 bits	open-collector				
5N54 S288(J, W)	SN74S288(J, N)	(32 W × 8 9)	three-state	25 ns	400 mW		
\$N54 S287(J, W)	SN74S287(J, N)	1024 bits	three-state				
3N54\$387(J, W)	\$N74S387(J, N)	(256 W x 4 B)	open-collector	42 ns	500 mW		
\$N54S470(J)	SN74S470(J, N)	2048 bits	open-collector				
SN54S471(J)	SN74S471(J, N)	(256 W x 8 BL)	three-state	50 ns	550 mW		
\$N54S472(J)	SN74S472(J, N)	4096 bits	three-state		·		
BN54S473(J)	SN74S473(J, N)	(512 W × 8 8)	open-collector	55 ns	600 mW		
BN64S474(J, W)	SN74S474(J, N)	4096 bits	three-state				
8N54S47 5(J, W)	SN74S475(J, N)	(512 W x 8 B)	open-collector	55 ns	600 mW		

256 BITS 22 WORDS BY 8 BITS) '\$188, '\$288	1024 BITS (256 WORDS BY 4 BITS '\$287, '\$387	2048 BITS) (256 WORDS BY 8 BITS) 'S470, 'S471	4096 BITS (512 WORDS BY 8 BITS) 'S472, 'S473	4096 BITS (512 WORDS BY 8 BITS) 'S474, 'S475
34 Vec 145 % 3	AO G 12	AD A 10 D20 VEC AD 8 2C D19 AD H AD C 3C D19 AD C AD D 4C D17 AD F AD E 5C D16 S2 D0 1 4C D18 S2 D0 2 1C D18 D0 R D0 3 8C D12 D0 6	AD A 10	00 1 0 1 20 1 20 1 20 1 20 1 20 1 20 1
Pin assignmi	ents for all of these memor	GND 1001 Div DOS	650 100 D11 00 S	001 9 5 14 007 007 19 6 7 15 004 00 11 1 5 5 7 16 004 00 13 5 7 16 004

1

ecription

These monolithic TTL programmable read-only memories (PROM's) feature titanium-tungsten (Ti-W) fuse links with ch link designed to program with a 100 microsecond pulse. These PROM's offer considerable flexibility for upgrading sisting designs or improving new designs as they feature full Schottky clamping for improved performance, ow-current MOS-compatible p-n-p inputs, choice of bus-driving three state or open-collector outputs, and improved hip-select access times.

high-complexity 2048- and 4096-bit 20-pin PROM's can be used to significantly improve system density for memories as all are offered in dual-in-line packages having pin-row spacings of 0.300 inch.

TEMMINARY DATA SHEET: data may be dahed at a later date,



†Integrated Schottky-Berrier diodeclamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

SERIES 54S/74S PROGRAMMABLE READ-ONLY MEMORIES

step-by-step programming procedure for the 'S188, 'S287, 'S288, 'S387, 'S470 through 'S475

- 1. Apply steady-state supply voltage ($V_{CC} = 5 \text{ V}$) and address the word to be programmed.
- 2. Verify that the bit location needs to be programmed. If not, proceed to the next bit.
- If the bit requires programming, disable the outputs by applying a high-logic-level voltage to the chip-select input(s).
- 4. Only one bit location is programmed at a time. Connect each output not being programmed to 5 V through 3.9kΩ and apply the voltage specified in the table to the output to be programmed. Maximum current out of the programming output is 150 mA. This current flows from the programmer into the PROM output.
- 5. Step VCC to 10.5 V nominal, Maximum supply current required during programming is 750 mA.
- Apply a low-logic-level voltage to the chip-select input(s). This should occur between 1 µs and 1 ms after VCC has
 reached its 10.5-V level. See programming sequence of Figure 2.
- 7. After the X pulse time is reached, a high logic level is applied to the chip-select inputs to disable the outputs.
- Within 1 µs to 1 ms after the chip-select input(s) reach a high logic level, VCC should be stepped down to 5 V at which level verification can be accomplished.
- The chip-select input(s) may be taken to a low logic level (to permit program verification). 1 µs or more after VCC reaches its steady-state value of 5 V.
- At a Y pulse duty cycle of 35% or less, repeat steps 1 through 8 for each output where it is desired to program a bit.
- OFE: Only one programming attempt per bit is recommended.

5V | | | 3.9 kΩ

LOAD CIRCUIT FOR EACH OUTPUT NOT BEING PROGRAMMED OR FOR PROGRAM VERIFICATION

FIGURE 1 - LOAD CIRCUIT

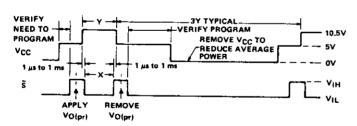


FIGURE 2 - VOLTAGE WAVEFORMS FOR PROGRAMMING



4

SERIES 54S/74S PROGRAMMABLE READ-ONLY MEMORIES

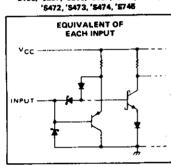
description (continued)

Data can be electronically programmed, as desired, at any bit location in accordance with the programming procedure specified. All PROM's, except the 'S287 and 'S387 are supplied with a low-logic-level output condition stored at each bit location. The programming procedure open-circuits Ti-W metal finks, which reverses the stored logic level at selected locations. The procedure is irreversible; once altered, the output for that bit location is permanently programmed. Outputs never having been altered may later be programmed to supply the opposite output level. Operation of the unit within the recommended operating conditions will not alter the memory content.

Active level(s) at the chip-select input(s) enables all of the outputs. An inactive level at any chip-select input causes all outputs to be off.

The three-state output offers the convenience of an open-collector output with the speed of a totem-pole output; it can be bus-connected to other similar outputs yet it retains the fast rise time characteristic of the TTL totem-pole output. The open-collector output offers the capability of direct interface with a data line having a passive pull-up.

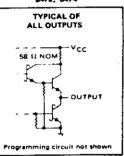
schematics of inputs and outputs 'S188, '\$287, '\$288, '\$387, '\$470, '\$471,



'S188, '\$387, '\$470 5743, '8475

TYPICAL OF -OUTPUT Programming circuit not shown

'\$287, '\$288, '\$471.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage free Note 11		7 V
Input voltage (see Note 1)		, , , 5.5 V
Officiate output voltage		. · , v
Operating free-air temperature range:	SN54S' Circuits = -00	3 C 10 123 C
	SN74S' Circuits	0°C to 70°C
Storage temperature range		5°C to 150°C

recommended conditions for programming the 'S188, 'S287, 'S288, 'S387, 'S470 through 'S475

		SN5	SN54S', SN74S'		
		MIN	NOM	MAX	UNI
	Steady state	4.75	5	5.25	T
Supply voltage, V _{CC} (see Note 1)	Program pulse	10	10.5	111	
	High level, VIH	2.4		·5	
Input voltage	Low level, VIL	0		5 5.25 5 11 [†] 5 0.5 circuit 6 1) 6 0.3 10 ³ 6 35]
Termination of all outputs except the one to be programmed		1	load cir Figure		
Voltage applied to output to be programmed, VO(pr) (see Note 2)		0	0.25	0.3	V
Duration of VCC programming pulse Y (see Figure 2 and Note 3)		98	100	103	μs
Programming duty cycle			25	35	%
Free-air temperature		0		55	°c

[†]Absolute maximum ratings

NOTES: 1. Voltage values are with respect to network ground terminal. The supply-voltage rating does not apply during programming.

2. The 'S188, 'S288, 'S470, 'S471, 'S472, 'S473, 'S474, and 'S475 are supplied with all bit locations containing a low logic level, and programming a bit changes the output of the bit to high logic level. The 'S287 and 'S387 are supplied with all bit outputs at a high logic level, and programming a bit changes it to a low logic level.

3. Programming is guaranteed if the pulse applied is 98 µs in duration.



SERIES 54S/74S PROGRAMMABLE READ-ONLY MEMORIES WITH 3-STATE OUTPUTS

recommended operating conditions

PARAMETER		'S2	8 7, '\$4	71		'\$288			470		
		MIN	NOM	MAX	MIN			'\$472, '\$		74	UNIT
Supply voltage, V _{CC}	Series 545	4.5	(5)	5.5		NOM	MAX	MIN	NOM	MAX	Div.
	Series 74S	4.75	(')		4.5	5	5.5	4.5	5	5.5	
High-level output current, IOH	Series 54S	+ 	73	5.25	4.75	5	5.25	4.75	5	5.25	٧
	Series 74S	+		2	↓ _		2			-2	
ow-level output current, IQL		 -		~6.5	⊢ ––		~6.5			-6.5	mA
perating free-air temperature, TA	Series 54S	-55		16			20			12	mA
	Series 746			125+	-55		125	-55			
ectrical characteristics over re	1 -4168 /45	0		70	0		70	-00		70	°c

electrical characteristics over recommended operating free air temperature range (unless otherwise noted)

<u> </u>	- CONSTRUCTER	TEST CON			SN548		T	SN74S		Ť
VIH	High-level input voltage	 		MIN	TYP#	MAX	MIN		MAX	UNI
VIL	Low-level input voltage		 	2			2			T .
VIK	input clamp voltage	VCC = MIN,	1.0.10			0.8			0.8	<u> </u>
۷он	High-level output voltage	VCC = MIN,	I _I = -18 mA V _{IH} = 2 V,	 		-1.2			-1.2	- -
		VIL ~ 0.8 V,	IOH = MAX	2.4	3.4		2.4	3.2		v
VOL	Low-level output voltage	VCC = MIN,	VIH = 2 V,	 -			 			Ľ
	Off-state output current,	V _{fL} = 0.8 V,	IOL - MAX	[0.5			0,5	v
OZH	high-level voltage applied	VCC = MAX, VO = 2.4 V	VIH = 2 V,							
ozu	Off-state output current,	VCC - MAX,		ļ		50			50	μА
	low-level voltage applied	Vo * 0.5 v	VIH = 2 V,	1		-50				
ľ	Input current at maximum			<u> </u>					-50	μА
tH	input voltage High-level input current	VCC = MAX,	V _I = 5.5 V			1 [,	mA
<u>, </u>	Low-level input current	VCC = MAX,	V ₁ = 2.7 V			25				1000
os	Short-circuit output current §	VCC - MAX,	V _I = 0.5 V			250			25	μА
		VCC = MAX		-30		100	-30		-250	μΑ
	•	VCC = MAX,	'S287		100	135		100		mA
c	Supply current	Chip select(s) at 0 V,			80	110			135	
		Outputs open, See Note 4	'\$471		10	155				mA
		See Note 4	'S472, 'S474		20	155			155	

switching characteristics over recommended ranges of TA and VCC (unless otherwise noted)

TEST CONDITIONS	ta(ad) (ns) Access time from address		fa(5) (ns) Access time from chip select (enable time)			φχζ (ns) Disable time from high or low level			וואט	
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TVDT	88.834	
C _L = 30 pF for te(ed) and te(S) 5 pF for tpx2;		42	75						_	
		42	65							rıs
		25	50							ns
		25	40					8	30	ns
RL = 300 Ω;	-	50		·				. 8	20	ns
See Figure 2, Page 13	 				20	40		15	35	ns
			70		20	35		15	30	ns.
		55	85		20	45				
		55	75		20	40				Ðέ
	C _L = 30 pF for le(ad) and t _B (S) 5 pF for tpXZ: R _L = 300 Ω; See Figure 2,	TEST CONDITIONS According to the second sec	Access time address Access time address	Access time from address MIN TYPT MAX	Access time from address Access time from address	Access time from address Access time from address Access time from address Access time hip select tens	Access time from address Access time from chip select (snable time)	Access time from address Access time from chip select (enable time) Display	Access time from address Access time from chip select (enable time) Access time from chip select (enable	Access time from address Access time from chip select (enable time) Disable time from high or low level



For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions
\$All typical values are at VCC = 5 V. TA = 25°C,
\$Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
\$AN\$45287 in the W package operating at free-air temperatures above 108°C requires a heat sink that provides a thermal resistance from NOTE 4: The typical values of ICC shown are with all outputs low.

PROGRAMMABLE READ-ONLY MEMORIES WITH OPEN-COLLECTOR OUTPUTS **SERIES 54S/74S**

recommended operating conditions

Ž,	Ī

1							_		•		7		
	PARAMETER			3188		' s	387, 'S	470	~	473, '\$4			7
1			MIN	NOM	MAX	MIN	NOM	MAX	MIN			UNIT	4
- 1	Supply voltage, V _{CC}	Series 54S	4.5	5	5.5	4.5				NOM	MAX		1
ľ	High-level guarante	Series 74S	4.75	5	5.25	4.75	-	5.5	4,5	5	5.5		7
ŀ	High-level output voltage, VOH			<u> </u>		4.75	5	5.25	4.75	5	5.25	1 "	1
ŀ	Low-level output current, IQL				5.5			5.5			5.5	v	1
1	Operating free-sir temperature, TA	Series 54S	 		20			16			12	 `	4
Ŀ	TA	Series 74S	-55		125	-55		125+	~55			mA	1
		341103 /43	0		70	0		70	 -		125	°c	ı
								;•1			70	1	1

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

 -	PARAMETER	o operating tree-air te		·		,,
VIH	High-level input voltage	TEST CONE	MIN TY	P\$ MA)	UNIT	
VIL	Low-level input voltage	- 		2	10.77	V
VIK	Input clamp voltage	- 			0.8	
		VCC - MIN,	II = -18 mA			<u> </u>
Юн	High-level output current	VCC = MIN, VIH = 2 V,	V _{OH} = 2.4 V		-1.2 50	+-
VOL	Low-level output voltage	VIL = 0.8 V	V _{OH} = 5.5 V		100	
li ·	Input current at maximum input voltage	VIL = 0.8 V.	VIH = 2 V,		0.5	v
IH	High-level input current	VCC - MAX,	V _I = 5.5 V			mA
IL_	Low-level input current	VCC - MAX,	V _I = 2.7 V		25	μA
		VCC = MAX,	V ₁ = 0.5 V		-250	μА
CC	Supply current	Chip select(s) at 0 V	'S387	80	110	
		Outputs open,	'S470	100	135	
		See Note 4		110	155	mA [
			'S473; 'S475	120	155	- 1

switching characteristics over recommended ranges of TA and VCC (unless otherwise noted)

ТҮРЕ	TEST CONDITIONS		^t e(ad) Access time from address			fe(S) Access time from thip select (enable time)		PLH Propagation dalay time iow-to-high-leval out- put from chip select (disable time)		vel out- select	UNIT
8N64S188		MIN	TYP#	MAX	MIN	TYP	MAX		TYP#	MAX	1
SN74S188			25	50		12	30				
3N54S387	CL = 30 pF.		25	40		12	25		12	30	ns_
BN74S387	RL1 = 300 Ω		42	75		15	40			25	ns
W64S470	RL2 = 600 Ω.		42	65		15	35		15	40	ns
N745470	See Figure 1,		50	80		20			15	35	ns
N54S473, SN54S475	Page 13		50	70			40		15	35	⊓s
N748743, SN748475			55	85		20	35		15	30	ns
717-37-43, SN74S475		 	55	 -+		_20	45		15	40	ns
V.			- 55	75		20	40		15	~	ns

conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

Typical values are at V_{CC} = 5 V, T_A = 25°C.

ENS4S387 in the W package operating at free-air temperatures above 108°C requires a heat sink that provides a thermal resistance from the typical values of f_{CC} shown are with all outputs low.



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SCHOTTKY[†] PROM'S

SERIES 54S/74S PROGRAMMABLE READ-ONLY MEMORIES

ES 1 AND 6)

E R TION	SEE PAGE
w	9
w	9
w	9
w	9

		
ICE IER ATION	SEE PAGE	
mW	20	
Wm	24	
mW D*mW	27	
mW D*mW	-	
TW TW	33	

N	SEE PAGE	
	39	

 Titanium-Tungsten (Ti-W) Fuse Links for Fast, Low-Voltage, Reliable Programming

All Schottky-Clamped PROM's Offer:
 Fast Chip Select to Simplify System Decode
 Choice of Three-State or Open-Collector Outputs
 P-N-P Inputs for Reduced Loading on
 System Buffers/Drivers

- Full Decoding and Chip Select Simplify System Design
 - Applications Include:
 Microprogramming/Firmware Loaders
 Code Converters/Character Generators
 Translators/Emulators
 Address Mapping/Look-Up Tables

			I	TYPICAL PER	FORMANCE
TYPE NUMBE	R (PACKAGES)	BIT SIZE	CONFIGURATION	ADDRESS	POWER
-55°C to 125°C	0°C to 70°C	(ORGANIZATION)	CONFIGURATION	ACCESS TIME	DISSIPATION
	SN74S1B8(J, N)	256 bits	open-collector	25 ns	400 mW
SN54S188(J, W)	SN74S288(J, N)	(32 W x 8 B)	three-state		
SN54S288(J, W)		1024 bits	three-state	42 ns	500 mW
N54S287(J, W)	SN74S287(J, N)	(256 W × 4 B)	open-collector		
SN54S387(J, W)	SN745387(J, N)		open-collector		550
SN54S470(J)	SN74S470(J, N)	2048 bits		50 ns	550 mW
SN54\$471(J)	SN74S471(J, N)	(256 W x 8 B)	three-state	 	
SN545472(J)	SN74S472(J, N)	4096 bits	three-state	- 55 ns	600 mW
	SN74S473(J, N)	(512W x 8 B)	open-collector		<u> </u>
SN54S473(J)		4096 bits	three-state	55 ns	600 mW
SN54S474(J, W)	SN74S474(J, N)	1	open-collector	7 55 113	
SN54S475(J, W)	SN74S475(J, N)	(512 W x 8 B)		_ 	

256 BITS	1024 BITS	2048 BITS	4096 BITS	4096 BITS
(32 WORDS BY 8 BITS)	(256 WORDS BY 4 BITS)	(256 WORDS BY 8 BITS)	(512 WORDS BY 8 BITS)	(512 WORDS BY 8 BITS)
'\$188, '\$288	'8287, '\$387	'S470, '\$471	'\$472, '\$473	'S474, 'S475
DO 1 IC D18 VCC DO 2 7C D18 5 DO 3 3 IC D18 5 DO 4 44 D19	AD 6 1: D16 VCC D15 AD H D14 32 AD 6 1: D14 32 AD A 1: D14 32 AD A 1: D14 D15 AD A 1: D15	AD A 10	AD A 1 () 18 AD 1	AD # 1 C

Pin assignments for all of these memories are the same for all packages

description

These monolithic TTL programmable read-only memories (PROM's) feature titanium-tungsten (Ti-W) fuse links with each link designed to program with a 100 microsecond pulse. These PROM's offer considerable flexibility for upgrading existing designs or improving new designs as they feature full Schottky clamping for improved performance, low-current MOS-compatible p-n-p inputs, choice of bus-driving three state or open-collector outputs, and improved chip-select access times.

The high-complexity 2048- and 4096-bit 20-pin PROM's can be used to significantly improve system density for fixed memories as all are offered in dual-in-line packages having pin-row spacings of 0.300 inch.

PRELIMINARY DATA SHEET: Supplementary data may be published at a later date.



†Integrated Schottky-Barrier diodeclamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

977

SERIES 54S/74S PROGRAMMABLE READ-ONLY MEMORIES

description (continued)

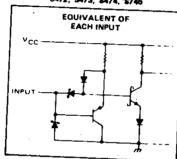
Data can be electronically programmed, as desired, at any bit location in accordance with the programming procedure specified. All PROM's, except the 'S287 and 'S387 are supplied with a low-logic-level output condition stored at each bit location. The programming procedure open-circuits Ti-W metal links, which reverses the stored logic level at selected locations. The procedure is irreversible; once altered, the output for that bit location is permanently programmed. Outputs never having been altered may later be programmed to supply the opposite output level. Operation of the unit within the recommended operating conditions will not alter the memory content.

Active level(s) at the chip-select input(s) enables all of the outputs. An inactive level at any chip-select input causes all

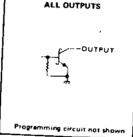
The three-state output offers the convenience of an open-collector output with the speed of a totem-pole output; it can be bus-connected to other similar outputs yet it retains the fast rise time characteristic of the TTL totem-pole output. The open-collector output offers the capability of direct interface with a data line having a passive pull-up.

schematics of inputs and outputs

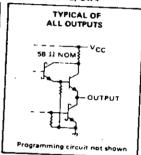
'5188, '\$287, '\$288, '\$387, '\$470, '\$471, '5472, '\$473, '\$474, '\$746



'\$188, '\$387, '\$470 \$743, '\$475 TYPICAL OF



'\$287, '\$288, '\$471, '8472, 'S474



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

COPPLY VOICAGE (See Note 1)															-,				
Input voltage Off-state output voltage Operation from a line of the line of th		•	•	٠.															7 V
Off-state output voltage Operating free-air temperature range:		Ċ		• •	-	٠	•	•	٠	٠	•	٠	٠	٠			• .		5.5 V
operating free-air temperature range:	SN54S' Circuits SN74S' Circuits	i			٠	•	•		•	•	•	٠	٠	٠	•	٠_:			5.5 V
Storage temperature	SN74S' Circuits				•	•	•	•	•	•	٠	•	٠	٠		-5.	5 C 1	io 1	25°C
Storage temperature range						Ċ			•	•	•	•	•	٠	•		0 C	to	70°C

recommended conditions for programming the 'S188, 'S287, 'S288, 'S387, 'S470 through 'S475

		SNE	45', SA	1745	
Supply voltage, VCC (see Note 1)		MIN	NOM	MAX	UNIT
	Steady state	4.75	- 5	5.25	1
Input voltage	Program pulse	10	10.5	111	1 V
	High level, VIH	2.4		- 5	
Termination of all currents	Low level, VIL	0		0.5	\ \
Termination of all outputs except the one to be programmed		See	load cir		
Voltage applied to output to be programmed, VO(pr) (see Note 2)		,	igure i		ĺ
CU Programming Dules V (see Eigens 2)		0	0.25	0.3	V
- Togramming duty cycle		98	100	103	μз
ree-air temperature			25	35	<u>*</u>
bsolute maximum ratings.		0		55	°c

Voltage values are with respect to network ground terminal. The supply-voltage rating does not apply during programming.
 The 'S188, 'S288, 'S470, 'S471, 'S472, 'S473, 'S474, and 'S475 are supplied with all bit locations containing a low logic level, and programming a bit changes the output of the bit to high logic level. The 'S287 and 'S387 are supplied with all bit outputs at a high logic level, and programming a bit changes it to a low logic level.
 Programming is guaranteed if the outse applied is 98 us in duration.

TEXAS INSTRUMENTS

step-by-st

1. / 2. 1

3. I

5. 1

10

NOTE: 0

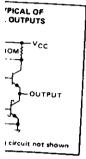
SERIES 54S/74S PROGRAMMABLE READ-ONLY MEMORIES

the programming procedure tput condition stored at each stored logic level at selected permanently programmed, t level. Operation of the unit

y chip-select input causes all

a totem-pole output; it can he TTL totem-pole output. Issive pull-up.

. 'S288, 'S471, 472, 'S474



ioted)

7 V 5.5 V 5.5 V -55°C to 125°C 0°C to 70°C -65°C to 150°C

19th 'S475

SN	45 , SN	745'	
IN	NOM	MAX	TINU
75	5	5.25	
10	10.5	117	1 🗸 1
.4		5	
0		0.5	V
ee	load cire	cuit	
_(igure 1) [- [
<u>0</u> _	0.25	0.3	V
8	100	103	με
	25	35	%
<u></u>		55	°C

g programming. ng a low logic level, and all bit outputs at a high step-by-step programming procedure for the 'S188, 'S287, 'S288, 'S387, 'S470 through 'S475

- 1. Apply steady-state supply voltage (VCC = 5 V) and address the word to be programmed.
- 2. Verify that the bit location needs to be programmed. If not, proceed to the next bit.
- 3. If the bit requires programming, disable the outputs by applying a high-logic-level voltage to the chip-select input(s).
- 4. Only one bit location is programmed at a time Connect each output not being programmed to 5 V through 3.9kΩ and apply the voltage specified in the table to the output to be programmed. Maximum current out of the programming output is 150 mA. This current flows from the programmer into the PROM output.
- 5. Step VCC to 10.5 V nominal. Maximum supply current required during programming is 750 mA
- Apply a low-logic-level voltage to the chip-select input(s). This should occur between 1 µs and 1 ms after VCC has
 reached its 10.5-V level. See programming sequence of Figure 2.
- 7. After the X pulse time is reached, a high logic level is applied to the chip-select inputs to disable the outputs.
- 8. Within 1 μ s to 1 ms after the chip-select input(s) reach a high logic level, VCC should be stepped down to 5 V at which level verification can be accomplished.
- The chip-select input(s) may be taken to a low logic level (to permit program verification). 1 μs or more after VCC
 reaches its steady-state value of 5 V.
- 10. At a Y pulse duty cycle of 35% or less, repeat steps 1 through 8 for each output where it is desired to program a bit.

NOTE: Only one programming attempt per bit is recommended



LOAD CIRCUIT FOR EACH OUTPUT NOT BEING PROGRAMMED OR FOR PROGRAM VERIFICATION

FIGURE 1 - LOAD CIRCUIT

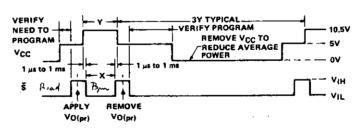


FIGURE 2 - VOLTAGE WAVEFORMS FOR PROGRAMMING

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 - DALLAS. TEXAS 75222

977



Bipolar PROM Cross Reference Guide

0.75 4415		NATIONAL	AMD	FAIRCHILD	HARRIS	INTEL	INTERSIL	M,M,I.	SIGNETICS	T.i.
SIZE AND GANIZATION	OUTPUT	MIL/COM	M = MIL C = COM	M = MIL C = COM	2 = M1L 5 = COM	M = MIL P = COM	M = MIL C = COM	MIL/COM -1 = SCHOTTKY	S = MIL N = COM	MIL/COM
256-Bit (32 x 8)	ос	DM54S188/DM74S188	AM27S08		HM1-7602 HM1-8256		IM5600	5330/6330	8223 82\$23	SN54188A/74188A SN54S188/74S188
16-Pin	T\$	DM54S288/DM74S288	AM27S09		HM1-7603		IM5610	5331/6331	82S123	SN54S288/74S288
1024-Bit (256 x 4)	ОС	DM54S387/DM74S387	AM27S10	93417 93416	HM1-7610 HM1-1024A	3601-1 3601	IM5603	5300/6300	82\$126	SN54S387/74S387
16-Pin	TS	DM54S287/DM74S287	AM27S11	93427 93426	HM1-7611 HM1-1024	3621	IM5623	5301/6301	825129	SN54S287/74S287
2048-Bit	ос	DM54S570/DM74S570		93436	НМ1-7620	3602	IM5604	5305/6305	82\$130	
(512 x 4) 16-Pin	TS	DM54S571/DM74S571		93446	HM1-7621	3622	IM5624	5306/6306	82\$131	
1096-Bit	ос	DM54S475/DM74S475		93438	HM1-7640	3604	IM5605	5340/6340	825140	SN54S475/74S475
(512 x 8) 24-Pin	TS	DM54S474/DM74S474		93448	HM1-7641	3624	IM5625	5341/6341	82S141	SN54S474/74S474
4096-Bit	ос	DM54S473/DM74S473				_		5348/6348		SN54S473/74S473
(512 x 8) 20-Pin	TS	DM54S472/DM74S472						5349/6349	:	SN54S472/74S472
4096-Bit	OC .	DM54S572/DM74S572*		93452	HM1-7642	3605		5352/6352	82S136	
(1024 x 4) 18 Pin	∦ js	DM64S673/DM74S573*		93453	HM1-7643	3625		5353/6353	82S137	

Note: All manufacturer's PROMs program differently . *Future products

OTAL DITC	PART N	UMBER	ORGANIZATION	NUMBER OF PINS	TEMPERATURE	MAXIMUM ADDRESS	MAXIMUM SUPPLY
OTAL BITS	PROM	ROM	ONGANIZATION	110MDEN OF 1MO	RANGE	ACCESS (tAA)	CURRENT (ICC)
256	DM54S188		32 x 8 OC	16	-55°C to +125°C	45	110
250	DM74S188		32 x 8 OC	16	0°C to +70°C	35	110
	DM54S288		32 x 8 TS	16	-55°C to +125°C	45	110
	DM74S288	!	32 x 8 TS	16	0°C to +70°C	35	110
1024	DM54S387	DM54S187	256 x 4 OC	16	-55°C to +125°C	60	130
1027	DM74S387	DM74S187	256 x 4 OC	16	0°C to +70°C	50	130
	DM54S287	DM75S97	256 x 4 TS	16	-55°C to +125°C	60	130
	DM74S287	DM85S97	256 x 4 TS	16	0°C to +70°C	50	130
2048	DM54S570	DM54S270	512 x 4 OC	16	-55°C to +125°C	65	130
2040	DM74S570	DM74S270	512 x 4 OC	16	0°C to +70°C	5 5	130
	DM54S571	DM54S370	512 x 4 TS	16	-55°C to +125°C	65	130
	DM74S571	DM74S370	512 x 4 TS	16	0°C to +70°C	55	130
4096	DM54S572		1k x 4 OC	18	-55°C to +125°C	75	140
4050	DM74S572		1k x 4 OC	18	0°C to +70°C	60	140
	DM54S573		1k×4 TS	18	-55°C to +125°C	75	140
	DM74S573		1k×4 TS	18	0°C to +70°C	60	140
4096	DM54S475	DM77S95	512 x 8 OC	24	-55°C to +125°C	75	170
,000	DM74S475	DM87S95	512 x 8 OC	24	0°C to +70°C	65	170
	DM54S474	DM77S96	512 x 8 TS	24	-55°C to +125°C	75	170
	DM74S474	DM87S96	512 x 8 TS	24	0°C to +70°C	65	170
8192		DM75S29	1k x 8 OC	24	-55°C to +125°C	90	160
0132		DM85S29	1k×8 OC	24	0°C to +70°C	70	160
		DM75528	1k x 8 TS	24	-55°C to +125°C	90	160

- New, Expanded Family of Standard, Low Power, Power Down, And Registered PROMs
- Titanium-Tungston (Ti-W) Fuse Links for Re-tlable Low-Voltage Full-Family-Competible Programming
- Full Decoding And Fast Chip Select Simplify System Design
- P-N-P Inputs for Reduced Leading On System Buffers/Drivers
- Each PROM Supplied With a High Logic Level Stored At Each Bit Location
- Applications Include:

Microprogramming/Firm Ware Loaders
Code Converters/Character Generators Translators/Emulators Address Mapping/Look-Up Tables

STANDARD PROMS

TYPE N	LIMBER	OUTPUT	017 SIZE	TYPH	AL PERF	PRMANCE
MEW TYPE NUMBER	OLD TYPE NUMBER	CONFIGURATION ⁴	(ORGANIZATION)	ACCESS		POWER
MEN ITTE HUMBER	0.01172.0000]	ADDRESS	SELECT	DISSPATION
T9734510 (J, N) [†]			1034 Bits	25 m	20 00	375 mm
TBP348A10 (J, N) [†]		Ω	(256W X 48)			3/0 000
T0P20042 (J, N)*		▽ .	4096 Biss	26.04	15.00	900 mW
TBP28545 (J, N)†		∇	612W X 885			500 mm
T9P24841 (J, N)*	6N74S476 (J, N)	∀	4086 Bits	40 m	20 ns	478 mW
TBP24SA41 LI, NIA	SN74\$477 (J, N)	Q	(1024W X 4B)			4/5 (300)
T8724981 (J, N)	BN745494 (J, N)	∇	\$192 Bits	45 m	20 ms	625 mW
TBP248AB1 (J, N)	9N748455 (J, N1	Q	(2048W X 48)	45 15	_~~	625 1994
T9720006 (J, N)	BN748478 (J, N)	∇				
TBP286ABS (J, N)	\$N748479 (J, N)	Q	8192 Sim	45 m	20 m	625 mW
TRP2852708 (J, N)	\$N7452708 (J, N)	∇	(1024W X 88)			
TBP20585 (J, N) [†]	1	\\ \nabla_{}	1	35 m	15 m	860 mW
TBP286186 (J, NI [†]		▽	16,364 Sits (2048W X 88)	36 ms ¹	16 m *	SUO milir

LOW POWER PROMS

TYPE N	UMBER	OUTPUT	BIT SIZE	TYPE	CAL PERF	DRMANCE
		CONFIGURATION'	(ORGANIZATION)	ACCESS	TIMES	POWER
NEW TYPE NUMBER	OLD TYPE NUMBER			ADDRESS	SELECT	DISSIPATION
			2048 Bits	45 ms	35 ns	300 mW
TBP28L22 (J, N) [†]		V	(256W X \$8)	45 76	35 (18	300 7771
TBP2BL42 LJ, NIT		▽	4096 Bits	60 ns	30 ns	250 mW
TBP28L45 (J, N)*		∇	(512W X 8B)			29U mm
TBP28LB8 (J, NIA	8N74L5478 (J, N)	▽	8192 Bits	2	35 m	350 mW
TBP28L85 (J, N) [†]		▽	(1024W X 88)	65 ms	30 №	275 mW
TBP28L166 (J, N) [†]		▽	16,384 Bits (2048W X 88)	6 5 ≈	30 ns	250 mW

NOTE - Electrical parameters for these devices are design gook only.

[≜] NOTE — These devices evaliable as full-temperature-range and as high-rel processed devices (use suffix MJ or NJ);
[†] Q = apon collector, ∇ = three state.

. 24 AND 28 .DARD, LOW-POWER, POWER-DOWN, REGISTERED .GRAMMABLE READ-ONLY MEMORIES

POWER DOWN PROMS

3 3	TYPE MANBE	A.A.DER	TUTTUO	BUT BUZE	2	Par bene	
Colone Bits	MEN TYPE INCREES	OLD TYPE MARKE	CONFIGURATION*	(ORGANIZATION)	ACCESS	TIMES	POWER
10					ADDATE	SELECT	DISCIPATION
	1 N T T T T T T T T T T T T T T T T T T		۵	4096 Bits			
Q (2001 61s, 36 m 36 m 10.00 to 10.00	TOP 200-45 (J. NJ)		Δ	(BRW X 88)	*	*	Mm 09/008
100404 X 881 36 m 36 m 36 m	TOCARONS (J. NUT		۵	6291 Gats	7 27	2	\$40,460 mW
(20000 x 22) 35 ns 35 ns				I DEM X BE			
	TEN 200 100 11, 11)T		D	(2048W × 64)	7 7	26 28	

	CARRE	CLITPLIT	617 6176			
W TVVE MARKER	GU TYPE MANAGER OLD TYPE MANAGER	CONFIGURATION*	CONFIGURATION CORE TO ADDRESS	CLOCK TO	TO ADDRESS FOW	POWER
				DUTFUT	SET UP TIME	OUTPUT SET UP TIME DISSIPATION
P 20000 (1, 11) *		D	4086 Bits			₩m 099
, (N. 1) season.		C	8162 Bits	-		
		>	(1024W X 88)	g g	ž R	900 mW
PROPERTY II. ALL		D	16,384 Bits			915
			(2048W × 88)			

After these devices are design goots andy.

The new 24 and 28 Series of monolithic TTL programmable read-only memories (PROMs) feature an expanded sheatlen of standard, low-power, power-down, and registered PROMs. This expanded PROM family provides the system feeigner with considerable flexibility in upgrading existing designs or optimizing new designs. Featuriny proven thenium-tungsten (T.F.W) has links with low-current MOS-compatible p-n-p inputs, all family members utilize a common programming technique designed to program each link with a 100-microsecond pulse.

for large PROM arrays. For systems requiring even higher levels of complexity and density, the 16,384-bit PROMs provide twice the bit density of the \$192-bit PROMs in 24-pin 600-mil-wide packages. All PROMs are supplied with a logichigh output level stored at each bit location. The programming procedure open-circuits Tr-W metal links, which teverus the stored logic level at selected locations. The procedure is irreversible; once altered, the output for that bit The new 4006-bit and £192-bit PROMs are offered in 24-pin 300-mil-wide packages, greatly improving system density coation is permanently programmed. Outputs that have never been altered may later be programmed to supply the possite output lovel. Operation of the unit within the recommended operating conditions will not alter the memory Active level(s) at the chip-select input(s) (S or S) anables all of the outputs. An inactive level at any chip-select input nume all eutputs to be off. On power-down PROMs, active leval(s) at the chip-enable input(s) (E or E) power up the bries and enables all of the outputs. An inactive level at any chip-enable input cause all the outputs to be off and the PROM to be in a reduced-power standby mode.

The three-state output offers the convenience of an open-collector output with the speed of a totem-pole output; it can be bus connected to other similar outputs, yet it retains the fast rise time characteristics of the TTL totem-pole MARKE. The open-collector output offers the capability of direct inserface with a data line heving a passive pull-up.

SERIES 24 AND 28 STANDARD, LOW-POWER, POWER-DOWN, REGISTERED PROGRAMMABLE READ-ONLY MEMORIES

18851118

PIN ASSIGNMENTS (TOP VIEWS)

	A S S S S S S S S S S S S S S S S S S S	A S S S S S S S S S S S S S S S S S S S
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THE SECTION OF SECTION	A A STATE OF	1922 BITE 1922

NC - No internal connection

. For those pline healing dual designations, the designation to the right of the urguin (f) applies only to the type numberial immediages fallowed by an asteriak (*) above the pineus drawing.

TEXAS INSTRUMENTS

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STANDARD, 10W-POWER, POWER-DOWN, REGISTERED PROGRAMMABLE READ-ONLY MEMORIES

EQUIVALENT OF EACH INPUT

schemetics of inputs and outputs

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2

PPCT

The standard PROM members of Series 24 and 28 offer the highest performance for applications requiring the uncom-premises speed of Echettity technology. The feet chip-select appear times allow additional decoding delays to occur without degrating speed performance.

PROPERTY PROPERTY

drive and speed parformance of bipoler technology and the reduced power dissipation recessary to implement effective INPERIOR. Additionally, tow-power PROMs other substantially reduced power dissipation over standard PROMs with To upgrade systems utilizing MOS EPROMs or MOS PROMs, the low-power PROM family offers the incressed output minimal speed paretty.

For power-ameltive systems requiring the speed performance of the standard PROM members as well as reduced system power dissipation, the power-down PROM members allow a 75% or better reduction in power assipation when disabled mille providing standard PROM speed performance when enabled. The power-down and power-up functions are enquenced to occur with the outputs at a high-impedance state. The enable (power-up) function provides adequate per-ferences to allow parents in a new attachment of the control of the c shoe to affew power-up to occur during the normal read occass time precluding any degradation in memory speed

For extensprogrammed pipelined systems the Series 24 and 28 registered PROM members offer the sysion designer reduced peckage count and improved performence by incorporating the pipeline weitter onto the PROM chip. Available in 4006-bit. 1182-bit and 16,384-bit densities, all registered PROMs are provided with synchronous and sayn-Aronaus output sontrols (G and G) allowing maxinum flexibility in data bus control.

hen power is first applied, the edge-triggered latch ier the synchrenous output control is cleared, and the hets are pleased in a high-impedance state. To defte, the address is set up, the synchronous outable, G(SYNC), is taken high, end a low-to-high into to be stored in the registers. That same transition the repirtor contents. If the synchronous output dition on the clock (C) input ceuses the selected ness the outputs to be enabled if seynchronous settles on the second of the second of the second on the second on the second of the s is charged and a new word addressed without affect nable is less at the time of a loss-to-high clock tran ition, the outputs will be disabled to the high-impedindo state. They may be disabled at any time by tak ng entent enemts G high

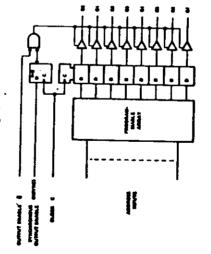
block diagram (positive logic)

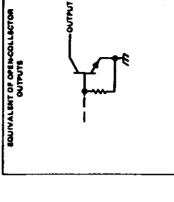
Ped 20 KII NOM 8 KII NOM

LOW-POWER PROMS
ALL OTHERS

Programming circuits not shown

EQUIVALENT OF 3-STATE OUTPUTS





-OUTPUT

absolute maximum ratings over operating free-air temperature range (unless otherwise notad)

130 ft NOM Se n NOM

LOW-POWER PROMS ALL OTHERS Programming cycuit not shown

Programming circuit net ahoum

2)	Supply voltage (see Note 1) Input voltage (S. S1, S2) (see Note 2) Off-state peak input voltage (S. S1, S2) (see Note 2) Off-state peak output voltage (see Note 2) Operating free-air temperature range: Full-temperature-range circuits (MJ) Storage temperature range -66°C te
11 11 4 4 1	11 11 4 4 1
	, S1, S2) (see Note 2) inge: Full:tamperal

NOTES 1. Voltage values are with respect to network ground terminal.

2. These ratings apply only under the conditions described in the pregramming precedure.

TEXAS INSTRUMENTS

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TEXAS INSTRUMENTS

STANDARD PROGRAMMABLE READ-ONLY MEMORIES WITH OPEN-COLLECTOR OUTPUTS ERIES 24 AND 28

nended operating conditions

and the same of th			TP-20EAB6	Target	S1 TBP24	177	2	PZ4EA10		
			MOM MAX	3		X	1	3	ž	Ĺ
	3	9.0	9.9	9,4	•	2	•	•	9.0	L
TO a second of the second of t	J, N	4.76	6 5.75	4.7	•	_	7.78	-	8.38 8.38	>_
HOP-land evenin vehicle, VOH			5.5			2			9.0	>
	3		12			9			2	Ŀ
	J, N		13			16			•	{
	3	*	126	\$		128	*		-28	٤
	7, 16	•	2	0		Q	0		۶	,

acteristics over recommended operating free-air temperature range (unless otherwise noted)

				LEVENCALL		·	L
É.,		Second Table	•	TEPZERABE	TEPTABAAI	TB-246A10*	
-		DI PORTO LEGI		MAIN TYP' MAX	MINE TYP? MAX MIN TYP! MAX MIN TYP! MAX	MAN TYP MAX	<u> </u>
3	High-lavel input values			2	~	7	Ŀ
	Law land input values			70	6.0	8	>
	Input clares values	VCC - MIN, Is18 mA		-1.3	-1.2	-1.2	Ŀ
		VOC - MM, VIN - 2 V. VO - 24 V	V0-24V	9	9	2	
		VIL - 0.8 V	V0 = 6.8 V	001	8	90,	<u> </u>
1		VCC . MINI, VIN - 2 V.	130	970	9.0	9.0	Ŀ
3		VIL - 0.8 V. IOL - MAX 3. N	N	970	970	9970	>
_	Input current or manifesture	VGC - MAX, VI - E.S V		-	-	-	1
×	High-four input current	VCC - MAX, VI - 2.7 V		20	15	2	1
J	Laterbard Ingus Currens	VCC * MAX. VI * 0.6 V		-340	-380	V* 082-	ş
1		Vac aut v	(14)	126	01-1-05	2	Ŀ
g İ			J, N	126 176	071 98	3/8	į
l							

For conditions shown so MMM or MAX, was the appropriate volve AM typical values are at $V_{QC}=8$ V, $V_{A}=26^{\circ}C_{c}$

itabing characteristics over recommended ranges of TA and VCC (unless otherwise noted)

		3	3			7		
į		Assess time from	Access time from the	ŧ	ŧ	Preparion date	į	
•		1	setes (enable time)	į	į	lime, lew-to-high-love sequent from ohip polar	time, two-to-high-to-ed	<u> </u>
		MAN TYP MAX	MAN TYP	XV	N. S.	Ł	MAX	
3		78	92	40		16	ş	
1,11		32	20	90		3.6	οc	2
Ž	. S	02 99	8	40		ደ	\$	ž
174	And Page 1-14	94 OP	8	40		8	\$	
7.0		9	00	×		8	S.	Z
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ra-range circuits (farituarly o deriosa are danigo genele enty. Ipotebura-congo obsudos (fermanty B4 Family), J end 34 desig Ĭ

TEXAS INSTRUMENTS

WITH 3-STATE OUTPUTS STANDARD PROGRAMMABLE READ-DNLY MEMORIES SERIES 24 AND 28

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		•	T0F24610*	•	T-200	M, 187	88 2708	1	E. 1	TIP 25686, TIP 2852 708 TIP 24681, TIP 24641	
PARAMETER		N	MIN NOM MAX MIN NOM MAX MIN NOM	MAX	MIM	MOM	MAX	NFR	MOM	MAX	
	TM1	4.5	10	5.5	4.5	•	6.6	4.5	•	6.5	?
Supply voltage, VCC	Z ,	4.76	40	6.25 4.75	4.76	9	6.25 4.76	4.76	•	6.25	•
	- FM			-3		e .	-3			-3	1
High-level output current, IOH	Z,			77			-3.2	L		-3.2	
	CM.			91			13			2	1
Low-level output current, IOL	2.7			16			12			91	
	3	-56		126	3		126	126 -66		176	<u>"•</u>
Operating free-sir temperature range	N Y	0		8	0		70	٥		2	_
electrical characteristics over recommended operating free-sir temperature range (unless otherwise noted)	ecommen	de pep	ersting	free e	r temp	Prettur	range	erun)	s other	wise no	Î
				ŀ				ŀ	L		L

PARAMETER PERT COMOITIONS TEPTAGEN						-	TEP24MII.		_	
High-level input voltage		PARAMETER	TEST CONDITIONS	-	TEF24610*	}	2484.	12024641		Ī
High-level input voltage High-level input voltage Low-level input voltage Low-level input cuttage VCC - MiN, VIH = 2V, Z.4 3.1 Z.4 3						F	86270s			
High-level input voltage					MIN TYP* MA	T MIM I	YP' MAX	MIN TYP' N	š	
High-level input voltage	ž	High-level input voltage			2	7		2	Н	٧
Input clamp voltage VCC = MIN, I = -18 m A	<u>۔</u> ح	Low-level input voltage			0		0.8		P. 0	^
High-tenti output voltage VCC=MiN,ViH=2V, Z4 3.1	¥	Input clamp voltage	VCC - MIN, It18 mA		·t-		-1.2	1	2	^
Construction output voltage VCC = MIN, VIH = 2 V, VC = MIN, VIH = 2 V, MIN = MIN	ě,	High-level output voltage	VCC - MIN, VIH - 2 V.			2.4	3.1	2.4 3.1		>
Off-lesis output current. VCC = MAX, VIH = 2 V, VO = 2.4 V BO BO BO Defi-lesis output current. VCC = MAX, VIH = 2 V, VO = 0.6 V — 60 — 60 — 60 Off-state output current. VCC = MAX, VIH = 2 V, VO = 0.6 V — 60 — 60 — 60 Input current at maximum. VCC = MAX, VIH = 0.5 V 1 1 1 Input current at maximum. VCC = MAX, VIH = 0.5 V — 780 — 780 — 780 High-level input current. VCC = MAX, VIH = 0.5 V — 780 — 780 — 780 Short-circuit. VCC = MAX, VIH = 0.5 V — 106 — 100 — 160 Short-circuit. VCC = MAX, VIH = 0.5 V — 106 — 100 — 100 Short-circuit. VCC = MAX MJ — 100 — 100 — 100 Supply current. VCC = MAX MJ — 100 — 100 — 100 Supply current. VCC = MAX MJ — 100 — 100 — 100 Supply current. VCC = MAX MJ — 100 — 100 — 100 Su	, o	Low-level output voltage	VCC - MIN. VIH - 2 V.		ïO		9.0		970	>
Off-state output current, VCC = MAX, VIH = 2 V, VO = 0.5 V -80 -	HZ0,	Off-state output current, high-level voltage applied	VCC - MAX, VIH - 2 V, V(0-24V	9		2		3	1
Input current ai maximum VCC = MAX, VI = 6.6 V 1 1 1 1 Input current air maximum VCC = MAX, VI = 6.5 V 26 26 26 26 High-level input current VCC = MAX, VI = 0.5 V -780 -780 -780 Short-enrent VCC = MAX J, N -20 -100 -10 -10 Supply current VCC = MAX J, N -76 -100 -30 -100 Supply current VCC = MAX J, N 75 126 130 -100	ומן	Off-state output current, low-lavel voltage applied	VCC - MAX, VIH - 2 V, V(0 - 0.5 V			3		3	1
High-level inout current VCC = MAX, Vi = 2.7 V 26 P 280	<i>-</i>	Input current at maximum input voltage					-			Į
Low-level input current VCC = MAX, V = 0.5 V -15 -100 -18 -100	Ī	High-level input current	VCC - MAX, VI - 2.7 V			9	2			₹
Short-sireui	=	Low-level input current	VCC - MAX, VI - 0.5 V		92-	0	-240		ş	1
Supply current VCC=MAX 1,N -20 -100 -20 -100 -20 -100 8 140		Short-circuit	2 4 7 4 7	TN1		91-0	-100	-16	8	1
Supply current VCC = MAX J, N 75 126 175 96 140	ő	Output current#	- 33 _A	J. N		02-0	-100	-30	8	
Supply current VCC NAAA 3, N 75 126 175 86 140				ſΝ			126 175		9	1
	ဒ္ဌ	Supply current	ACC - MAX	Z	32		128 176		\$	Į.

¹ All typical values are at V_{CC} = 8 V, T_A = 28°C. §Not more than one putput should be shorted at a time, and duration of the short circuit should not exceed one been

switching characteristics over recommended ϵ anges of TA and VCC (unless otherwise noted)

TBP24S10 MJ CL = 30 pF See Page I-14 MJ CL = 5 pF See Page I-14 MJ CL = 5 pF MJ MJ CL = 5 pF MJ MJ MJ MJ MJ MJ MJ M						(4)A			(8)4,			ZXd		
MJ C = 30 pF See Page 1-14 C = 50 pF See Page 1-14 See Page	BdA1		TEST C	ONDITIONS	į	and lines	<u>.</u>	Įł	i (englis) :			4	1	3
MJ C ₁ = 30 pF 35 35 36 16 36 36 36 36 36 36					Z		XY.	1	Ţ	MAX	NIN	TYP	MAX	
1, N C ₁ = 30 pF 35 30 40 16 30 30 30 30 30 30 30 3		3				36			92	35		18	36	£
10r te(A)	TB#24510*	z	C 30 pF			35			8	9		16	96	₹.
MJ	TBP24581		to (€(A)			46	ይ		R	3		8	9	8
10r (PXZ 1-5 pF 1-14 40 60 20 40 30 30 40 30 40		3	and t _e (S).			ş	28		8	9		92	9	\$
10r teX2 45 70 20 40 20 40	18724541	z	CL - 5 PF			Q¥	3		2	8		8	8	2
	TBP28586		10 texz			46	۶		8	4		8		1
	TBP2852708					,	•		۱ ا	}		۱ ا	ı	<u>'</u>

- Electrica perameters for trees conscious en comp. posts any. NOTE: - MJ designates full-temperatura-tanga circulta (formerly 6e Family), J and N designate

TEXAS INSTRUMENTS

MBS 24 AND 28 MBARD PROGRAMMABLE READ-ONLY MEMORIES IN 3-STATE OUTPUTS

	_	7			-			F	77.75		
		3	MOR	W.	4	HOM	MAX	MIT	MOM	MAX	
78		4.8	•	818	4.4	9	9.9	4.6	•	979	Ŀ
N'T		7,	•	1.25	4.76	-	\$.26	4.76	•	6.26	<u> </u>
71				2			2			-3	Ľ
N. F. HOD. Turning sections of	,			-3.2			-3.2			-3.2	į
CN.				16			2			2	į
1, N	ź			16			16			91	É
CMI		#		136	91-		126	-64		126	
J, N	2	0		30	0		2	0		20	,

operating free-eir temperature range (unless otherwise noted)

PARAMETER	TEST COMOCTIONS	<u>-</u>	TIPZERAG	•	T.	TBP26666	Ē	TBF288166*	3
			MAN TYP* MAX		T ME	TAME 14	1 1994 L	INN TYP! MAX MIN TYP! MAX	
edition teach teach right g			2		~		ŧ		۸
Sandard Inquit values				3		3	L	8	2
adespe despe trake	VCC - MIN. 1, 18 mA			F		-			F
dage index payagge W	VCC - MIN, VIH - 2 V.		24 3.1		22	3.1	3	ā	>
L. Landard augus voluge	VCC - MIN, VIM - 2 V.			3		570		9.5	>
Offices duties author (6)	VCC - MAX, VIH - 2 V, VO - 24 V	V 25 - 0		8		3		8	1
Off-amo naque current, It territoris unkapo applica	VCC - MAX, VM + 2 V, VQ - 6.5 V	A 970 - 0		7		8		2	1
elingen printer unarjeste og skildet printer	A 5'8 - IA 'XYW - 20A			-		+		-	ŧ
Mightenet Input current	VCC - MAX, VI - 2.7 V			2		æ		æ	4
Lawtons Input summe	VCC - MAX. VI - 0.8 V			9K-		-280		-260	4
Brant-streak	A PORT OF THE	[78]	-16	-1001-	Ę	81-	==	-100	
esignes sucranel	*GE - ===	1, #	-30	-100 -20	92	-100	Ŗ	-100	Ę
	*****	3	106		11	110		8	Ŀ
	- 30 ₄	3, 14	\$		11	110		8	{

. are at VCC * 6 V. TA * 26°C.

S) then son outbut chould be charted at a time, and duration of the chart circuit should not exceed one second

ferticities over recommended ranges of TA and VCC (unless otherwise noted)

	=======================================		2	ž	z
_		¥ X			
7	Office the	TYP MAX MIN TYP MAX	12	12	12
		3		Ц	
		MAX			
3	ij		2	=	#
1 1	3				
	1	X			
3		TYP	×	20	×
	į				
	THET COMBITIONS		R 300 G.	A-1-4	
	20 TBBT		7 - To		No. Water
	Ē				*

ters for states devices are design gasts andy.

M. designates full-temperature-range chaults (formarly 64 Funity), J and N designates
 M. Fornityi.

TEXAS INSTRUMENTS

SERIES 24 AND 28 LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES WITH 3-STATE OUTPUTS

recommended operating conditions

			TBF281.22*		TETAT	42°. TB	TBP28L42", TBP28L46"		THESELBE	=	
PARAMETER		3	MOM	MIN NOM MAX MIN NOM MAX MIN	2	100	MAX	NW	MOM	MAX	
	3	*	-	9.9	4.6	•	1.6	914	•	8.6	^
Supply volume, VCC	7.	4.7	-	\$.26	5.26 4.76	1	6 6.76 4.75	4.76	•	1.26	_
	₹			7			-1			7	1
High Level output purrent, 10H	z			-1.6			-1.4			-14	Ŀ
	3			•						•	1
Lanctarel author current, 40L	₹.									-	
	3	35		126	\$		128	*		ž	٠
Operating free-elr temperature range	7.7	۰		۶	0		ደ	٥		۶	凵
			,			1			4	Manager and the state of the st	į

electrical charactaristics over recommended operating free-sir temperature range

High-level input voltage Low-level input voltage Low-level input voltage Voc = MiN, Vi = -18 mA High-level output voltage Voc = MiN, Vi = 24 Voc = MiN, Vi = 27 Low-level output voltage Voc = MiN, Vi = 27 Voc = MiN, Vi = 27 Voc = MAX, Vi = 27 Whigh-level input current Voc = MAX, VI = 27 Whigh-level input current Voc = MAX, VI = 27 Whigh-level input current Voc = MAX, VI = 27 Whigh-level input current Voc = MAX, VI = 27 Whigh-level input current Voc = MAX, VI = 27 Whigh-level current Voc = MAX, VI = 27 Whigh-level current V						TBF284.42*	\vdash			
High-level input voltage		PARAMETER	TEST CONDITIONS	-	TB#281.22*	TEPZBLAZ		-	,	5
High-level input voltage					MIN TYP' MAS		AX MA	LAB	ž	
Low-level input datage	2 2	High-level indut voltage			2	2		3		>
Input clamp voltage	5	Low-level Input voltage			8		3		870	۸
High-lavel output voltage Voc=MiN, ViH=2V, 2.4 3.1	¥	Input clemp voltage	VCC - MIN, Is18 mA		7		~		-13	H
Off-state output voltage VCC = MINI, VH = 2 V. VC = MINI, VH = 2 V. VC = MOX. MOX. <td>ş</td> <td>High-level output voltage</td> <td>VCC - MIN, VIH - 2 V.</td> <td></td> <td></td> <td>'</td> <td>4</td> <td>1.1</td> <td></td> <td>></td>	ş	High-level output voltage	VCC - MIN, VIH - 2 V.			'	4	1.1		>
Off-class output current, Ingle-band votices applied Voc = MAX, VIH = 2 V, VO = 0.5 V = 60	, o	Low-tevel output voltage	VCC - MIN, VIH - 2 V,		ro		-		3	>
Description output current, VCC = MAX, VIH = 2 Y, VC = 0.5 V —80 —80 —80 —90	3	Off-state output current, high-level voltage applied	VCC - MAX, VIH - 2 V. V	0-24V	3		2		3	
Heput current at maximum V _{CC} = MAX, V ₁ = E.S 1 1 1 1 1 1 1 1 1	ğ		VCC - MAX, VIH - 2 V. V	0 - 0.B V	7		3		*	,
High-level Input current Voc. MAX, V = 2.7 V 25 25 25 25 25 25 25	<u>-</u>	Input current at maximum Input voltage	VCC - MAX, V1 - 5.5 V			_	-		-	1
Low-level input current VCC = MAX, V = 0.6 V -100	Ē	High-level Input current	VCC - MAX, VI - 2.7 V		~		×		8	- 1
Supply ourtent VCC=MAX 1.N -10 -100-10 -100 -10 -10 -10 -10 -10 -1	ڃٰ[Low-level input current	VCC - MAX, V1 - 0.6 V		2.				Ŗ	- 1
Supply ourset VCC - MAX 1.1.N 60 86 80 60	1	Short-circuit	Vor = MAX	3			8 1		<u> </u>	1
Supply ournit VCC - MAX J.N 60 86 80 60	8	output dument	3	z				1	3 2	I
	इ	Supply current	Vcc-MAX	2 Z	3		+	8	18	1

f par conditions shown as MiN or MAX, use the appropriets value specified unde

4 All system values are at V.C. = 8 V, T.A. = 28 °C. Byee more than one output should be shared at a time, and duredon of the shart eleval should not exceed one excend

switching characteristics over recommended ranges of TA and VCC (unites otherwise noted)

	_	_	-,			_
3		2			_	_
•	X				8	£
	£	*	=	*	3	2
	3					
11	TYP MAX				136	8
Access then them did enter (could item)	Į,	8	8	8	.8	3
Įł	1	L				
1	TYP MAX MIN				176	Ş
*		ş	\$	8	8	8
	3					Ц
DITIONS				R 600 fl.		
TEST CONDITIONS			, 30 př	for Se(A)	C, . 5 pf	for texz
		3	Z		3	z
TVM			TB-20, 22°	TBP28L42*		TBP28L86

• Electrical parameters for these devices are design gode only.

NOTE: Not designates full-temperature-range circuits (formerly 64 Femily), J and N designate
74 Femily).

934344944		F	-96787-98-	•	Ш	TBF281 106*		
			100	HOM MAX	3	NOM MAX	MAX	
	3	9.4	•	1.6	4,5	•	1.6	<u> </u>
30. ······	J, N	4.76	9	1.25	94.7	•	£.26	>
	3			٦,			-۱	ŀ
	J, N			4.1-			-1.2	Į
	3			•			•	•
	J, N			•			•	•
	74	99-		128	99-		126	٠.
	J, N	0		92	0		2	,
								*

			TREZBLAG		TBP 284.166*	•	
	STATE OF THE PARTY		HANN TYPE I	MAX	HIN TYP	MAX	5
High-level input voltage			2		2		>
Later towel input wellings				3	'	0	>
ingest efeme vertage	V _{CC} = MIN, I ₁ = -18 mA			-1.2		-1.2	-
Mightered event welness	VCC - MIN, VIH - 2 V. VIL - 0.8 V. IQH - MAX		2.4 3.1		2.4 3.1		>
Lamines augus velage	V _L = 0.8 V, I _{OL} = MAX			9.0		0.6	>
Offices earth current, high-land velops explied	A 72 - 0A 'A 2 - 14A 'XY# - 30A)-24V		2		8	1
Offices surput surrent, leavited vetage applied	A90-0A'A2-MA'XVM-30A)-0.5 V		9		7	1
began carrent at menimum ingut valtage	A 9'9 - 1A 'XVW - 30A			1			į
High-bord ingut aurrent	A 2'2 - 1A 'XY# - 30A			æ		32	₹
Lear-level ingut current	VCC - MAX, Vt - 0.5 V		ľ	-280		-260	į
Thert-circuit	2	791	-10	-100	-10	-100	1
author content	. 30.	N'f	-10	-100	-10	-100	1
	2422	79	3		2		1
	- 30) A	J, N	2	Г	2		£

nded ranges of TA and VCC (unless otherwise noted)

				3			3			,		
E	TEST CONDITIONS		į	Access then from	ļ	Įł	uses tenden time!	į		-	1	3
			H	TYP	MAX MM TYP MAX MM TYP MAX	MM	TYP	MAX	N	T.	MAX	
-96786				*			8			×		2
288. 188°	G 6 pf for tox2 See Page 1-15	20 Page 1:58		3		. '	Я			×		2

TEXAS INSTRUMENTS

POWER-DOWN PROGRAMMABLE READ-ONLY MEMORIES WITH 3-STATE OUTPUTS

recommended operating conditions

				Therese Therese.				-		•	
1111											į
PARAMETER		3	101	NOM MAX MAN NOM MAX MAN WOM	ĭ	3	¥	3	3	3	
	3	4.6	-	2	ş	•	9.6	1.1	•	1	3
Supply veltage, VCC			•	3	1.26 4.76	-	12	4.76	•	1.25	
				٦			7			7	1
history current, IOH				1			7			-3.2	•
			١				!			7.	
	3			=			=			1	1
Less tend output outrant, 10L]			2			=			2	
	•	1		2	3		175	7		2	
Operating free-sir temperature range	2	ľ		8	°		ደ	0		8	
									-	-	4

High-level Input current; VCC = MIN, VIH = 2 V, VO = 0.8 VCC = MIN, VIH = 0.8 VC					1			F	
High-level Ingust voltage									1
High-tend input voltage				TRET COMOLTIONS	- BARABL	The Zames	The San Lead	٦	5
High-level input coltage VCC = MIN, I = -18 mA					MAN TYP' MAX			3	١
High-level input rollings					,	7	7	>	_
VGC=MIN, I_1=-18 mA -1.2 -1.2 -1.2 VGC=MIN, VIH=2V 2.4 3.1 2.4 3.1 VIL=0.8 V, IQH=MAX 0.8 0.8 0.8 VIL=0.8 V, IQH=MAX 0.8 0.8 0.8 VIL=0.8 V, IQH=MAX 0.8 0.8 0.8 VGC=MAX, VIH=2 V, VQ=2.4 V 0.8 0.0 0.0 VGC=MAX, VI=2.7 V -3.0 -3.0 -3.0 VGC=MAX, VI=0.5 V -10 -10 -10 VGC=MAX, VI=0.5 V -10 -26 -10 VGC=MAX, VI=0.5 V -10 -26 -10 VGC=MAX, VI=0.5 V -10 -20 -10 VGC=MAX, VI=0.5 V -10 -20 -10 VGC=MAX, VI=0.5 V -10 -26 -10 VGC=MAX, VI=0.5 V -10 -26 <th>月</th> <th>1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1</th> <th>Input voltage</th> <th></th> <th>0.0</th> <th></th> <th></th> <th>7 8.0</th> <th></th>	月	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Input voltage		0.0			7 8.0	
VCC=MIN, I_1=-18 mA 2A 3.1 2A 3.1 2A 3.1 VCC=MIN, VIH=2 V. 2A 3.1 2A 3.1 2A 3.1 VCC=MIN, VIH=2 V. 0.8 0.8 0.8 VCC=MAX, VIH=2 V. VC=0.8 V -80 -80 VCC=MAX, VIH=2 V. VC=0.8 V -80 -80 VCC=MAX, VIH=2 V. VC=0.8 V -80 -80 VCC=MAX, VI=2.7 V -70 -70 -70 VCC=MAX, VI=0.5 V -10 -10 -10 VCC=MAX 10 -10 -10 -10 VCC=MAX 1.0 -10 -10 -10	VII.	Lose terrel				-1-			,
VCC=MIN, VIH=2V, 2A 3.1 <	;	Inout cler		VCC = MIN, ij = -18 mA	715			+	1
VCC = MIN, VH = 2 V. 0.5 0.5 VIL = 0.8 V, IOL = MAX. 80 80 VCC = MAX, VIH = 2 V, VO = 0.5 V -80 -80 VCC = MAX, VIH = 2 V, VO = 0.5 V -80 -80 MVCC = MAX, VIH = 2 V, VO = 0.5 V 1 1 VCC = MAX, VIH = 2.7 V -70 -76 -76 VCC = MAX, VIH = 0.5 V -100 -10 -76 VCC = MAX 1, N -20 -100 -70 VCC = MAX 1, N -20 -100 -20 -70 VCC = MAX 1, N -20 -100 -20 -70 -70	Ş	High Love		VCC - MIN, VIH - 2 V.	2.4 3.1		- 1	-	,
Off-state output current, Injury VCC = MAX, VIH = 2 V, VO = 2.4 V 60 60 60 Diff-state output current, Injury VCC = MAX, VIH = 2 V, VO = 0.5 V — 60 — 60 — 60 Injury output current of maximum VCC = MAX, VI = 2.7 V 2.5 C 2.5 C 2.5 C High-level input current of vCC = MAX, VI = 0.5 V MA — 160 — 160 — 160 Bioch-climit output current of vCC = MAX, VI = 0.5 V MA — 160 — 160 — 160 Shopby VCC = MAX VCC = MAX 1, N — 20 — 160 — 160 Shopby VCC = MAX VCC = MAX 1, N — 20 — 160 — 160 Shopby Pocc = MAX VCC = MAX 1, N — 20 — 160 — 160 Shopby Pocc = MAX VCC = MAX — 160 — 160 — 160 — 160	\ \ \	Losting	seuport voltage	VCC - MIN, VIH - 2 V.	\$10	6.6		1	,
VCC=MAX.V ₁₁ =5.V.YO=0.5 V 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Į,	Off-custs	output current,	VCC - MAX, VIH - 2 V, VO - 2.4 V	3				4
Non-store variety and section 1 1 1 1 1 1 1 1 1	129	Off-state	output current.	VCC-MAX VIH - 2 V, VO - 0.5 V	8				1
Imput voltage 76 76 76 High-level input current V _{CC} = MAX, V ₁ = 2.7 V -760 -720 Low-level input current V _{CC} = MAX, V ₁ = 0.5 V -760 -16 -100 Short-circuit V _{CC} = MAX J, N -20 -100 -10 Supply Power Up V _{CC} = MAX J, N -20 -100 -20 Supply Power Up V _{CC} = MAX J, N -20 -100 -100 -100	1	-1	ment at maximum	V _{CC} - MAX, V _I - 6.5 V				*	1
High-band input current VCC = MAX, V = 0.5 V Low-band input current VCC = MAX, V = 0.5 V Low-band input current VCC = MAX J, N -20 -100 -20 100 20 100 20 100 20 100 20 100 20 2	- [Input vo	200	> C > > +	*			_	4
Short-chrost logot current VCC = MAX	크	T T	M input current	VCC - MAA. V O. V.	-260				1
Short-circuit VCC = MAX J, N -20 -100 -20 -100 -20 -100	4		a Input current				-18	힐	1
Supply Power Up V.C.* MAX 12 12	8	Short ch		<u>, </u>			-30	힐	H
VCC - MAX	1	1	Poster 1 to		001	110	ē	Ť	1
	8			Vcc = MAX	12	12	=	1	ļ

switching characteristics over recommended ranges of TA and VCC (unless otherwise noted) 4 AM typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}C$. Since the first character of the short character are expert should not second and seconds.

•	Obserbte time Libert	MAN TYP MAN	12 m	12 75	12	
3	Access three from chip	MAN TYP MAX MIN TYP MAX MAN TYP MAK	*	36	36	
3	Assess then from	NAM TYP MAX	36	35	36	Aly.
	TiONS		3m o	for Pare 1:14		speed veries are s
:	TEST CONDITIONS		CL - 30 pF for	Tela and telti-	CL - SpF for texz	The the second of these devices are design gods only.
	W A			19728746	T80280168	

circuits (formatly 84 Femily). J and N dasig NOTE: MJ designates full-: 74 Family).

ERIES 24 AND 28 EGISTERED PROGRAMMABLE READ-ONLY MEMORIES WTH 3-STATE OUTPUTS

led operating conditions

400 0000		•	- T- 20 7.4		=	T-28ABG	•	F	TBP28R 166*	•	1
		NAME	14044	MAX	MIN	MOM	MAX	3	3	XAX	3
	3	9"7	•	8.8	4.6	•	6.5	4.6	9	6.5	-
SS . Tempera	J, N	4.76	•	1.25	4.78	•	6.26	4.76	•	2	>
	3			~			7			٦	Ĺ
HD, 'was sense and the	J, N			?			-3.2			-3.2	É
	78			10			¥.			19	Ŀ
Market Contract, 101.	7			91			-			z	Ę
sets puter width high, tagCH		98		Ĭ	92			R			2
sek pulse midth lens, t _{eriCL})		8			8			8			Z
Mires senso dem. I _{se} (A)		æ			8			8			2
tip calent source time, t _{ay} (g)		0			0			6			ž
Africa heat sime, the A		0			0			٥			2
to enter head three, types		8			۰			9			ŧ
	774	99-		126	3		126	3		126	
	N'Y	0		8	a		8	0		ደ	2

temperature range (unless otherwise noted)

			•	,						
		(anothernos		.97V924EL		TBPZBRB6*	.98	13F2BR166*	.991	
	The state of the s			MAN TYP* MAX		BEN TYP* MAX MEN TYP* MAX	741	HAN TYP	* MAX	•
Į,	High-land Input volume			2		2		2		۸
ķ	Lessional Input values				3		3		0.0	>
MA	Separt elemb vellage	NOC - MIN, Is 18 mA			-1.2		<u>r1-</u>		-1.2	>
Š	state total sugari untage	VCC - MIN. VIH - 2 V.		2.6 2.5		2.4 3.1		22	_	^
į		VCC - MM', VIN - 2 V.	n#		0.6		9.0		0.6	1
4		VIL - 08 V. IOL - MAX	- N 'F		9.0		3		0.5	>
B	Offices expet current, high-land values expiled	VCC - MAX, VIN - 2 V, VO - 24 V	24.4		3		3		3	4
형	Off-spee august surrent, ten-land veltage applied	A 970 = 0A'A 2 = MA'XW = 50A	V 8.0		3		ş		8	٧n
4	Imput correct of manifesters Imput voltage	VGC - MAX, VI - 6.5 V			-		-		-	ΨΨ
M	High-lovel Input marrant	VCC - MAX, VI - 2.7 V			92		92		8	∀π
1	Lewierd Input current	VCC - MAX. VI - 0.5 V			-280		-260		-250	٧×
1	Dierreimeit	7 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4	7	-15	-10018	-16	-100	-16	-100	
3	surper current b	VCC - mm.	N'F	-30	-100 -20	-30	-100	~30	-100	§
1		****	7	110	_	120		110	0	1
,	The second second		N'f	110		130		110	0	m.

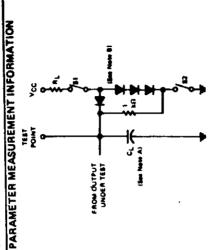
TEXAS INSTRUMENTS

SERIES 24 AND 28 REGISTERED PROGRAMMABLE READ-ONLY MEMORIES WITH 3-STATE OUTPUTS

switching characteristics over recommended ranges of TA and VCC (unless otherwise noted)

types TBP28R46*, TBP28R86*, TBP28R166*

* Electrical and switching parameters for these devices are dealen goals only.



NOTES. A. C. Includes probe and lig capeties.

6. All slodes are 1N916 or 1N3064.

LOAD CIRCUIT

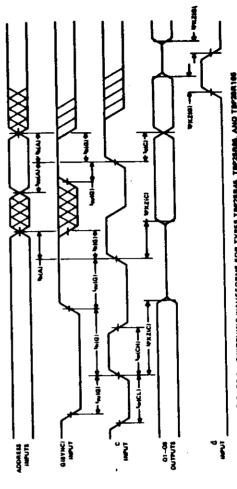


FIGURE 1 - SMITCHING MAVEFORMS FOR TYPES TBF2SRAS, TBF2SRAS, AND TBF2BR196

TEXAS INSTRUMENTS

-

SERIES 24 AND 28 PROGRAMMABLE READ-ONLY MEMORIES

SERIES 24 AND 28 PROGRAMMABLE READ-ONLY MEMORIES

secumended conditions for programming

PARAMETER		1	177	XX	TES
Seast-state supply vehicles, Voc.		4.6	1	8.8	>
	HA	77		•	>
Company state company	VIL	•		0.6	•
E3 sed E4 legut veltage (where appropriete)	VIR	2.4		9	>
recommend		٥	9	0.5	>
	Voltage, VCC(pr)	£ 76	Э	6.26	>
Anante untern geranden perte (see Flavo 2)	Pulse width, Is.	1000		2000	1
L	Duty syste		38	36	×
	Volumes, VS(pr)	97.0	(10	=	>
Control of a series of the ser	VIL		4		
	Volume, Vo(pr)	16.31	6(1)	E'11 (11)	^
	Wise time, 1,	(0)		(60)	ž
Confer brokersund broke from 1 force 20	Pulse width, Sur	3	<u>8</u>	100 1000	1
-	VIL	۰		0.5	
Shadoward PROM verify elects pulse valdos	'watch)	Ŀ	8		nξ
Present parameters. Ta		٥		3	٠,

poby emp programming instructions (see Figure 2)

- Address the word to be programmed, apply $\delta V \pm 10\%$ to V_{CC} and active levels to all phip select (S and \overline{S}) or chip enable (E and \overline{S}) inputs.
- . Verify the status of a bit location by checking the output level. For registered PROMs a clock must be applied to the clack pin to verify the output level.
- Ingress VCC to VCC(pr) with a minimum current capability of 200 milliamperes.
- Apply Vs.(pr) to all the S. E or G inputs. I, < 15 mA.
- Connect all outputs, except the one to be programmed, to a logic low level (0 < V_{IL} < 0.5 V). Only one bit is programmed at a time.
- Apply the output programming pulse for at least 98 microseconds. Minimum current capability of the programming supply should be 200 milliamperes.
- After terminating the output pulse, disconnect all outputs from V_{IL} conditions.
- Reduce the voltage at \$, E or 6 inputs to VIL.
- Regions VCC to standy-state voltage and verify output status. Note that for registered PROMs, a clock must be applied to the stock input pin to verify output status.
- Repeat steps 3 through 9 for each bit location that requires programming.
- Verify accurate programming of every word after all words have been programmed using VCC values of 4.5 add
 8.5 wolts, Note that registered PROMs must be clocked to verify the output condition.

Š E > ! . ž A Verify present Î 2 1 ¥ T 0 4 See Note 5) Surface -Verify CLOCK (REGISTERED PROMS ONLY) VCC PROGRAMMING SELECT OR ENABLE PROGRAMMING PULSE ADDRESS HAPUTS PUTTO PROGRAMMING PULSE VERIFY

FIGURE 2 – TIMING DIAGRAM AND VOLTAGE MAVEFORMS FOR PROGRAMMING SEQUENCE NOTE: The extent to be programmed may be forted to zero velts after the transition to Volge) at the E Indus has begun.